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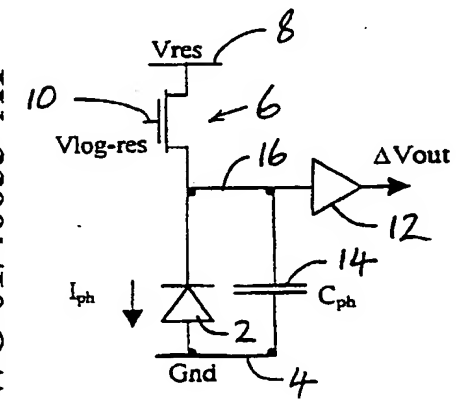
(54) Title: PHOTODETECTOR AND METHOD FOR DETECTING RADIATION



(57) Abstract: In a photodetector, a photodiode and a capacitor are coupled between a sensing node and a ground voltage line, and a MOS transistor is coupled between the sensing node and a reference voltage line. Initially, the capacitor is charged so that the sensing node voltage is greater than a transition voltage and a predetermined gate voltage is applied to switch the transistor off. During a sampling time, the capacitor initially discharges through the photodiode, the discharge current being dependent on the intensity of radiation incident on the photodiode, until the sensing node voltage falls to the transition voltage. If the sensing node voltage falls to the transition voltage during the sampling time, the transistor enters its weak inversion operation domain and the current through the photodiode can flow through the transistor such that the sensing node voltage varies logarithmically with the radiation intensity. At the end of the sampling time, a readout circuit coupled to the sensing node generates an output signal dependent on the sensing node voltage, and the photodetector is reset by recharging the capacitor before the start of another sampling time.

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Photodetector and Method for Detecting Radiation

The invention relates to a photodetector, or optoelectronic sensor, and a method for detecting radiation.

State of the Art

To date, two principles for detecting radiation in solid-state image sensors prevail: charge-coupled-device (CDD) sensors and metal oxide semiconductor (MOS) sensors. CCD sensors are limited in dynamic range, because of the limited capacitance under the charge collecting gate of the CCD. Many applications, however, require a wide dynamic range signals of up to 140dB in terms of the relationship between minimum and maximum detectable. In MOS sensors, particularly in active pixel sensors (APS) which use CMOS technology, this problem can be solved by using a detector producing a logarithmic response to the incident light intensity see reference [Cha 1]. But such a logarithmic response detector disadvantageously has a response time inversely proportional to the light intensity. This is a problem because many applications require a high readout speed over the whole dynamic range, including for very low radiation intensities, where classical logarithmic response detectors have an extremely long response time see reference [Vie 2].

In a classical logarithmic response photodetector, as shown schematically in figure 1, photodiode 100 is connected to the channel of a MOS transistor 102. The gate 104 of the transistor is connected to its drain. Light impinging on the photodiode generates a photocurrent I_{ph} that is converted into a voltage over the MOS transistor. For typical photocurrents from femtoamperes to nanoamperes, the transistor operates in weak inversion and the voltage across the transistor V_{GS} (gate to source voltage) can be calculated using formula 1.

$$V_{GS} = \frac{kT}{\kappa q} \ell n(\frac{I_{ph}}{I_0}) + V_{TH}$$ Formula 1

In formula 1, κ is a process dependent transistor parameter, I_0 is the drain current at the onset of the weak inversion operation of the transistor and V_{TH} is the transistor's threshold voltage. kT/q is roughly 26mV at ambient temperature (k = Boltzmann's constant, T = temperature and q = electronic charge).

To understand the response time of a logarithmic detector the equivalent circuit, or incremental model, of figure 2 can be considered. In this equivalent circuit, the loading MOS transistor is replaced by a transconductance 106, whose value $g_{m\log}$ depends on the photocurrent I_{ph}, and the photodiode is replaced by an equivalent current source 107 which drains current from the transconductance 106. See formula 2.

$$g_{m\log} = \frac{\delta I_{ph}}{\delta V_{DS}} \propto I_0 \exp(V_{DS})$$ Formula 2

In formula 2, V_{DS} is the drain to source voltage across the transistor.

Thus at a given light intensity, the response time of the detector to a small change of the photocurrent is given by formula 3, where C_{ph} is the capacitance of the photodiode capacitor 108. This response time becomes excessively long for very small photocurrent values.

$$\tau = \frac{C_{ph}}{g_{m\log}}$$ Formula 3

Integrating CMOS photodetectors overcome the problem of the response time by performing a reset of the accumulated photocharge after readout. But since the response of these sensors is linear to the incident light intensity, such integrating sensors have a dynamic

range limited by the voltage swing on the integration capacitance on the one hand, and the minimum detectable signal due to readout noise on the other hand.

Summary of the Invention

The invention provides a photodetector, or optoelectronic sensor, and a method for detecting light as defined in the appended independent claims. Preferred or advantageous features of the invention are defined in dependent subclaims.

In order to realise a photodetector providing both fast response time and high dynamic range, the invention may advantageously provide a combination of aspects of the integrating and logarithmic photodetectors.

In a preferred embodiment of the photodetector, a photodiode (or other zone of semiconductor material for collecting photogenerated charges) and a capacitance are coupled in parallel between a ground line and a sense node, and the channel of a MOS transistor is coupled between the sense node and a supply voltage line. Usually, the capacitance may be the parasitic capacitance of the photodiode (or the zone of photosensitive semiconductor material) and neighbouring components. A low capacitance is usually desirable as this improves circuit sensitivity.

In an initial reset, the capacitance is charged so that the sense node voltage is above a transition voltage as described below.

After resetting, the transistor gate voltage is set so as to block, or switch off, the transistor, and the photodetector enters a sampling phase. Current flows through the photodiode in relation to the radiation intensity incident on it, which initially discharges the capacitance so that the sense node voltage falls substantially linearly in relation to the radiation intensity. At this stage no current flows through the transistor but if and when the sense node

voltage falls to the transition voltage, the transistor enters its weak inversion operation domain. The photocurrent can then flow through the MOS transistor channel and so the sense node voltage begins to fall logarithmically in relation to the radiation intensity.

The transition voltage is equal to the gate voltage applied to the load transistor during sampling minus the transistor threshold voltage. Advantageously, the transition voltage can therefore be set by controlling the gate voltage or by adapting the threshold voltage by technological parameter adjustment.

In more general terms, it will be appreciated that the invention allows the load transistor to be used in both its normal mode, during which the photodetector response is linear, and in its weak inversion mode, during which the photodetector response is logarithmic. In addition, the invention ensures a smooth transition between these modes and makes it possible to choose the level at which the transition occurs.

In a further preferred implementation, the transition voltage may be varied during operation, such as during a sampling phase or between sampling phases, by varying the gate voltage of the load transistor. This may advantageously allow even more flexible control of the linear/logarithmic response of the photodetector and may allow the detector's dynamic range to be further increased.

An important feature of preferred embodiments of the invention is therefore to be able to choose, or control, the sense node voltage at the beginning of the sampling phase and to choose, or control, the gate voltage of the load transistor during the sampling phase. These voltages determine the behaviour of the circuit and the transition from linear to logarithmic behaviour.

Thus, the invention may advantageously provide a photodetector and a method of detecting radiation which provide a much greater dynamic

range and speed of response than conventional detectors. In particular, the invention may achieve a logarithmic response over part of its dynamic range without the drawback of increasing response time for low light intensities.

In a preferred embodiment, the sense node voltage after the initial reset may conveniently be close to the circuit supply voltage, achieved by coupling the sense node to the supply voltage line, for example by controlling the load transistor gate voltage to switch on the load transistor channel.

In this document, the invention is embodied using a photodiode as a radiation sensitive element. In practice, however, a variety of types of component comprising zones of semiconductor material suitably doped to generate charges in response to incident radiation could be used.

In this document, examples are given in which the supply voltage is greater than the ground voltage. This could be reversed and the described circuits modified accordingly to create dual versions of the circuits, as the skilled person would be aware.

In practice, a photodetector of the invention may have a dynamic range of 120dB or more, such as 160dB. In tests, such circuits have achieved a measured dynamic range of about 200dB.

The photodetector and method of the invention may advantageously find many applications, in particular for viewing applications with high contrast in the viewed scene. Such applications may include surveillance applications, soldering control, welding control or automotive driving assistance applications. Other applications would readily be apparent to the skilled person.

Description of Specific Embodiments

Specific embodiments and the best mode of the invention will now be

described by way of example, with reference to the drawings, in which;

Figure 1 (prior art) shows a conventional logarithmic photodetector circuit;

Figure 2 (prior art) shows an equivalent circuit, or incremental model, of the circuit of figure 1;

Figure 3 shows a photodetector circuit according to a first embodiment of the invention;

Figure 4 is a timing diagram for the circuit of figure 3;

Figure 5 shows a photodetector circuit according to a second embodiment of the invention;

Figure 6 shows a photodetector circuit according to a third embodiment of the invention, suited for integration into one or two dimensional devices;

Figure 7 is a plot of the output of a photodetector embodying the invention against incident optical power, illustrating linear and logarithmic response regions; and

Figure 8 is an enlargement of a portion of figure 7, showing the transition between the linear and logarithmic response regions.

A schematic of a photodetector according to a first embodiment of the invention is drawn in figure 3.

A photodiode 2 is connected between a ground voltage line 4 and the channel of a MOS Transistor 6 (Source terminal). The source terminal is also connected to a readout circuit 12 with high input impedance, in order to sense the voltage on the sensing node 16 between the photodiode and the transistor and to generate a corresponding output voltage ΔV_{out}. The drain terminal of the transistor 6 is coupled to a voltage V_{res}. A capacitance 14 of value C_{ph} is connected in parallel with the photodiode. This capacitance may not, in practice, be a separate component but may be formed of all the parasitic capacitances of the sense node 16.

The circuit operates as follows. A readout cycle, as illustrated in the timing diagram of figure 4, begins with the resetting 200 of the voltage across the photodiode and the capacitance (i.e.the sense node voltage, termed V_{signal} in figure 4) to a reset voltage V_{res}. This can be done by applying a voltage 202 higher than the reset voltage plus the threshold voltage V_{TH} of the MOS (V_{res} + V_{TH} in figure 4) to the gate terminal. The MOS is then conducting, and regardless of the photocurrent, the photodiode and capacitor will be set to the reset voltage.

The gate terminal is then switched to a predetermined voltage $V_{log-res}$ within an analogue voltage range. The predetermined voltage is higher than the ground voltage of the photodiode plus the threshold voltage of the transistor (Gnd + V_{TH}) and equal to or lower than the reset voltage (V_{res}). The MOS transistor is now blocked, or switched off. The circuit now enters a sampling interval 204 during which integration of the radiation incident on the photodiode occurs. The photocurrent then discharges the capacitor 14 connected to the sense node 16. This is the integrating mode of operation of the detector, and the sense node voltage decreases at a rate 208 which is initially linearly proportional to the impinging light intensity. If the impinging light intensity is high enough to discharge the sense node capacitance below the gate voltage minus the threshold voltage ($V_{log-res}$ - V_{TH}), the detector enters a logarithmic mode 210. In this mode, the MOS enters its weak inversion operation domain, and the photocurrent can flow through the MOS channel. The gate-source voltage (V_{GS}) generated by the photocurrent is then described by formula 1 above. The signal on the sense node is thus compressed in the logarithmic mode by the logarithmic law of formula 2.

After a predetermined sampling time, the voltage at the sense node is read 212 by the readout circuit to produce a corresponding output signal ΔV_{out}, and the photodiode is reset again 200 by applying a high voltage to the gate terminal of the MOS transistor.

In an alternative embodiment, as illustrated in figure 5, instead of switching the load transistor 6 to reset the circuit, the gate of this transistor can be set to a predetermined analogue voltage value, between V_{res} and V_{TH}, and a second MOS transistor 40 can be used as a reset switch. As shown in figure 5, the gate of the photodetector transistor 6 in this embodiment can conveniently be coupled to V_{res} at the drain of the transistor. However, selection of the predetermined gate voltage valve within the range described determines the point at which the circuit response changes from linear to logarithmic, and so may advantageously be selected or varied to tailor the circuit for different applications.

The circuit of figure 5 has the advantage that no voltage greater than the supply voltage V_{res} is needed. This is of particular benefit in an integrated circuit implementation where, using this embodiment, no voltage greater than the supply voltage would be needed on the chip. By contrast, in the embodiment described in figures 3 and 4 a voltage $V_{res} + V_{TH}$ greater than V_{res}, the supply voltage, was required to raise the sense node to V_{res} during the reset phase.

The photodetector of the invention can be realised with very few components, and is therefore suited for integration in 1 or 2 dimensional arrays (line sensors or image sensors). Preferably a two dimensional array of photodetectors may be realised by integrating the output amplifier or buffer (readout circuit) directly with the detector for each pixel as for active pixel sensors (APS). This can be done most easily by adding a source follower transistor 42 and a select transistor 44 to the detector, as drawn in figure 6 in conventional manner. This allows information to be extracted from a pixel of a 1 or 2 dimensional array of photodetectors. In figure 6 the supply voltage is conventionally termed VDD (voltage drain-to-drain).

In the described embodiments, MOS transistors have been shown. In practice pMOS or nMOS transistors or equivalent components may be

used as appropriate.

In the embodiments of figures 3 and 5 described above, a fixed transistor gate voltage has been applied during the sampling, or integration, phrase of operation. Advantageously, the gate voltage can be selected to vary the point of the change from linear to logarithmic response of the detector. Further advantageously, however, the gate voltage may be varied during or between sampling phases, for example by varying the gate voltage linearly from its maximum (V_{res} + V_{TH} in figures 3 and 4) to minimum (Gnd + V_{TH} in figures 3 and 4) values, or by varying it under active control or using a feedback control system, to further modify the linear/logarithmic compression curve and, preferably, to further increase the detector's dynamic range.

Figure 7 illustrates the measured performance of a circuit embodying the invention in terms of the sense node voltage measured at the end of the sampling time plotted against incident radiation power. The circuit is termed LINLOG™. The plot clearly shows the linear response 300 at low radiation powers and the smooth transition 302 to a logarithmic response 304 at high radiation powers. Figure 8 enlarges the low radiation power portion of the plot of figure 7, more clearly showing the linear region 300 and the transition region 302.

References:

[Cha 1] United States Patent Appl. No.: 373872 Savvas. G Chamberlain Sept 25 1984

[Vie 2] Oliver Vietze "Active pixel image sensors with application specific performance based on standard silicon CMOS processes" p.97ff Dissertation submitted to the Swiss federal institute of technology Zürich, Switzerland. Diss. ETH no. 12038 1997

Claims

1. A photodetector comprising;

a zone of a semiconductor material suitably doped to collect photogenerated charges, coupled between a ground voltage and a sensing node;

a capacitance coupled in parallel to the zone of semiconductor material, between the ground voltage and the sensing node;

a transistor coupled at its source and drain between the sensing node and a supply voltage; and

a means for applying a predetermined voltage to the gate of the transistor;

in which, if the capacitance has been charged so that the magnitude of a voltage at the sensing node is greater than a transition voltage magnitude and a predetermined gate voltage is applied so that the transistor is non-conductive, then a photocurrent of a magnitude dependent on the intensity of radiation incident upon the zone of semiconductor material flows therethrough, discharging the capacitance and causing the sensing node voltage to vary substantially linearly with the photocurrent magnitude until the sensing node voltage reaches the transition voltage, and thereafter the transistor becomes conductive and the photocurrent generates a sensing node voltage which changes substantially logarithmically with the photocurrent magnitude.

2. A photodetector according to claim 1, in which the transistor is a metal oxide semiconductor (MOS) transistor.

3. A photodetector according to claim 1 or 2, in which the zone of semiconductor material is a photodiode.

4. A photodetector according to any preceding claim, in which the capacitance comprises a parasitic capacitance of the zone of semiconductor material.

5. A photodetector according to any preceding claim, comprising a sampling control means for resetting the photodetector by recharging the capacitance at the start of a sampling time and controlling a readout circuit coupled to the sensing node to generate an output dependent on the sensing node voltage at the end of the sampling time.

6. A photodetector according to any preceding claim, in which the photodetector is reset by controlling the means for applying a predetermined voltage to the transistor gate to apply a gate voltage which makes the transistor conductive and allows current to flow through the transistor to charge the capacitance.

7. A photodetector according to any of claims 1 to 5, comprising a reset transistor coupled between the reset voltage and the sensing node, and in which the photodetector is reset by applying a gate voltage to the reset transistor which makes it conductive and allows current to flow through the reset transistor to charge the capacitance.

8. A photodetector according to any preceding claim, comprising a readout circuit for generating an output signal dependent on the sensing node voltage.

9. A photodetector according to claim 8, in which the readout circuit is a source follower circuit.

10. A photodetector according to any preceding claim, implemented in an active pixel sensor.

11. A photodetector according to any preceding claim, in which the gate voltage means can apply a gate voltage which varies over time.

12. A photodetector according to any preceding claim, in which the photodetector's response to radiation can be varied by controlling the sensing node voltage at the end of the reset phase and the transistor gate voltage during the sampling time.

13. A photodetector according to any preceding claim, in which the transistor operates in its normal mode, and is blocked, before the sensing node voltage reaches the transition voltage, and operates in a weak inversion mode thereafter.

14. A photodetector array comprising a plurality of photodetectors as defined in any preceding claim.

15. A method for detecting radiation in a photodetector in which a zone of a semiconductor material suitably doped to collect photogenerated charges is coupled at a sensing node to the channel of a transistor, comprising the steps of;

resetting the photodetector by charging a capacitance coupled in parallel to the zone of semiconductor material so that the magnitude of the sensing node voltage is greater than a transition voltage magnitude;

applying a predetermined gate voltage to the transistor to block, or switch off, the transistor channel;

sampling incident radiation intensity by illuminating the zone of semiconductor material to generate a photocurrent, which discharges the capacitance such that the sensing node voltage changes substantially linearly in relation to the photocurrent, while the transistor operates in its normal mode, until the sensing node voltage reaches the transition voltage; and

after the sensing node voltage reaches the transition voltage, continuing to illuminate the zone of semiconductor material and generate the photocurrent while the transistor operates in a weak

inversion mode so that the sensing node voltage changes substantially logarithmically in relation to the photocurrent.

16. A method according to claim 15, in which the transistor is a MOS transistor.

17. A method according to claim 15 or 16, in which the capacitance comprises a parasitic capacitance of the zone of semiconductor material.

18. A method according to any of claims 15 to 17, comprising the step of generating an output signal based on the sensing node voltage at the end of a predetermined sampling time.

19. A method according to any of claims 15 to 18, comprising the step of varying the transistor gate voltage with time in order to control the response of the photodetector.

20. A method according to claim 19, in which the transistor gate voltage is varied during radiation sampling.

21. A method according to any of claims 15 to 20, comprising the step of controlling the sampling node voltage at the end of resetting in order to control the response of the photodetector.

22. A photodetector comprising a zone of a semiconductor material, suitably doped to collect photogenerated charges, and a capacitance coupled in parallel to one end of a channel of a transistor at a sensing node, the photodetector being controllable to operate such that during a reset phase the capacitance is charged so that the magnitude of the voltage at the sensing node is greater than a transition voltage magnitude, and during a sampling phase a predetermined gate voltage is applied to the transistor and radiation incident on the zone of semiconductor material generates a photocurrent which causes the magnitude of the sensing node voltage to fall, the transistor operating in a normal mode when the

magnitude of the sensing node voltage is greater the transition voltage magnitude, and operating in a weak inversion mode when the magnitude of the sensing node voltage is less than the transition voltage magnitude.

23. A photodetector comprising a zone of a semiconductor material, suitably doped to collect photogenerated charges, and a capacitance coupled in parallel to one end of a channel of a transistor at a sensing node, the photodetector being controllable to operate such that during a reset phase the capacitance is charged so that the magnitude of the voltage at the sensing node is greater than a transition voltage magnitude, and during a sampling phase a predetermined gate voltage is applied to the transistor and radiation incident on the zone of semiconductor material generates a photocurrent which causes the magnitude of the sensing node voltage to fall substantially in proportion to the radiation intensity until it reaches the transition voltage magnitude, and to fall substantially logarithmically in relation to the radiation intensity thereafter.

24. A method for detecting radiation , comprising the steps of;

providing a photodetector comprising a zone of a semiconductor material, suitably doped to collect photogenerated charges, and a capacitance coupled in parallel to one end of a channel of a transistor at a sensing node; and

operating the photodetector such that during a reset phase the capacitance is charged so that the magnitude of the voltage at the sensing node is greater than a transition voltage magnitude, and during a sampling phase a predetermined gate voltage is applied to the transistor and radiation incident on the zone of semiconductor material generates a photocurrent which causes the magnitude of the sensing node voltage to fall, the transistor operating in a normal mode when the magnitude of the sensing node voltage is greater the transition voltage magnitude, and operating in a weak inversion mode

when the magnitude of the sensing node voltage is less than the transition voltage magnitude.

25. A method for detecting radiation, comprising the steps of;

providing a photodetector comprising a zone of a semiconductor material, suitably doped to collect photogenerated charges, and a capacitance coupled in parallel to one end of a channel of a transistor at a sensing node; and

operating the photodetector such that during a reset phase the capacitance is charged so that the magnitude of the voltage at the sensing node is greater than a transition voltage magnitude, and during a sampling phase a predetermined gate voltage is applied to the transistor and radiation incident on the zone of semiconductor material generates a photocurrent which causes the magnitude of the sensing node voltage to fall substantially in proportion to the radiation intensity until it reaches the transition voltage magnitude, and to fall substantially logarithmically in relation to the radiation intensity thereafter.

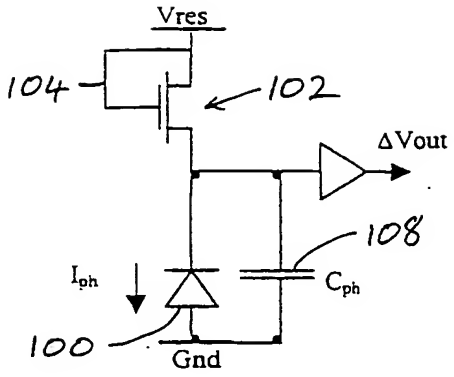

Figure 1.

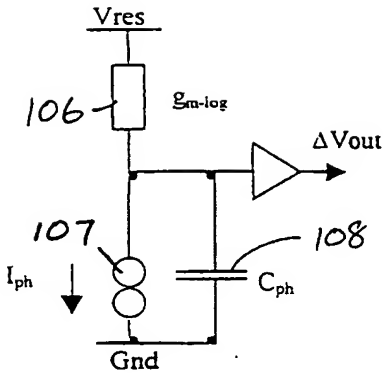

Figure 2

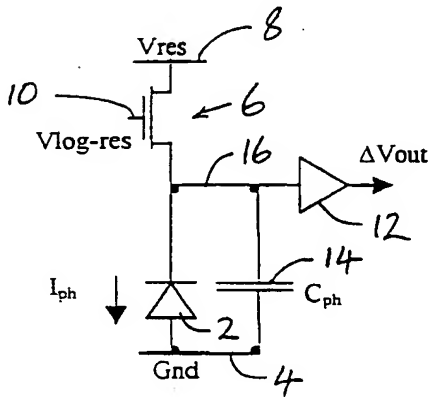

Figure 3

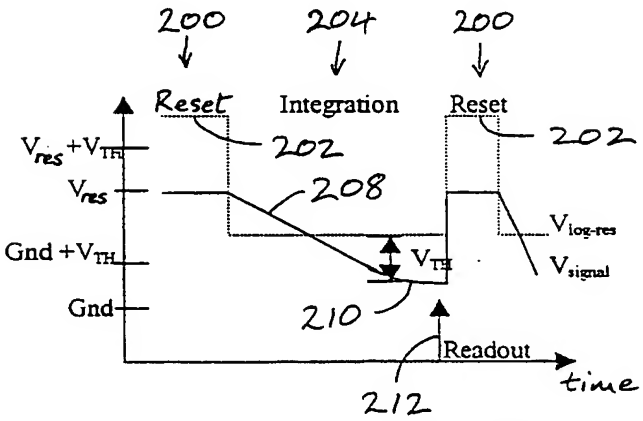

Figure 4

..... Gate Voltage

— Sense Node Voltage

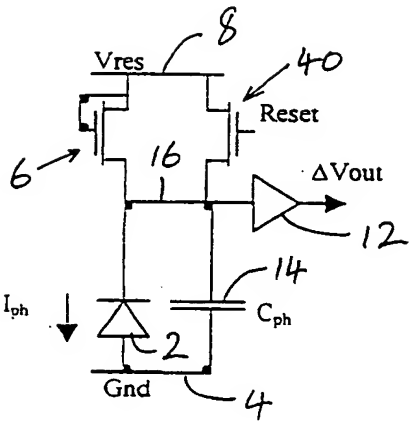

Figure 5

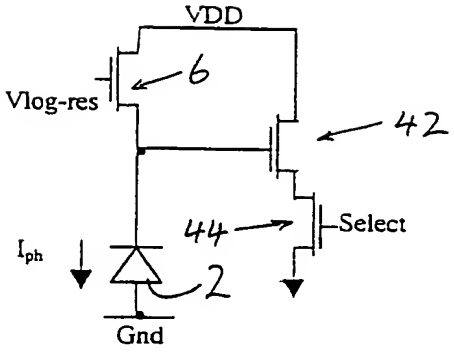

Figure 6

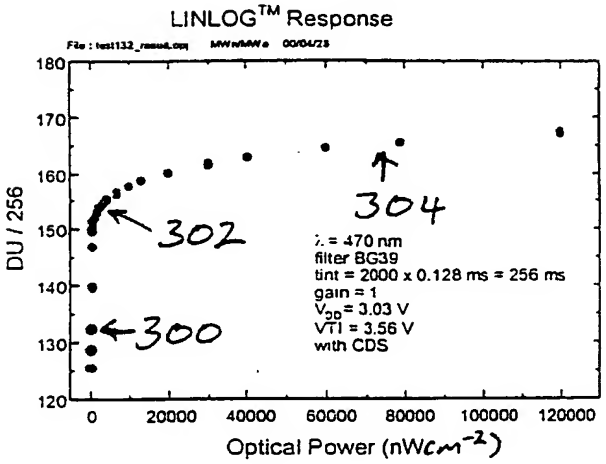

Figure 7

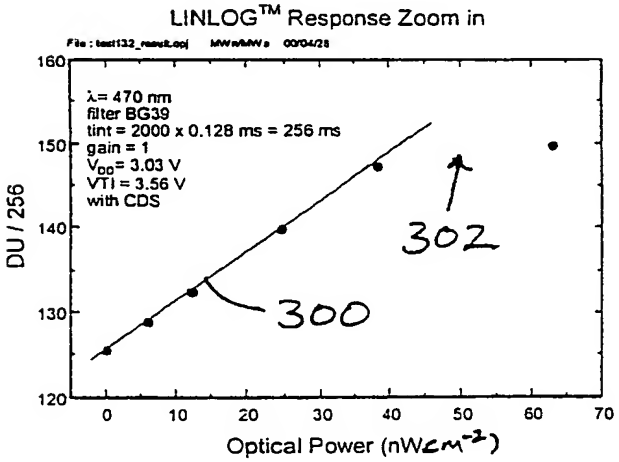

Figure 8

INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP 00/13114

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G01J1/46

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G01J H04N H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 936 866 A (SEITZ PETER ET AL) 10 August 1999 (1999-08-10) claims 1,6	1-3,15, 22-25
A	FR 2 751 823 A (ZHU YI MING) 30 January 1998 (1998-01-30) page 2, line 12-27	1-3,15, 22-25
P,X	WO 00 30343 A (BREISCH JAMES ;CONNOLLY KEVIN (US); INTEL CORP (US); MORRIS TONIA) 25 May 2000 (2000-05-25) claims 1-4	1-3,15, 22-25

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
17 May 2001	28/05/2001

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International Application No
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